VERTICAL CHARGE TRANSFER ACTIVE PIXEL SENSOR

This Patent Application claims priority to the following U.S. Provisional

5   Patent Application, herein incorporated by reference:

60/450,089, filed February 2, 2003.

10   BACKGROUND OF THE INVENTION

(1) FIELD OF THE INVENTION

15   This invention relates to an active pixel sensor using a deep N well or P

well to achieve vertical charge transfer.

(2) DESCRIPTION OF THE RELATED ART

20   U.S. Pat. No. 6,501,109 to Chi describes an active CMOS pixel sensor

with a p well within a deep n well.

U.S. Pat. No. 6,001,667 to Saitoh et al. describes a method of manufacturing a semiconductor detector for detecting light radiation showing a p well within a deep n well.

5   U.S. Pat. No. 5,600,127 to Kimata describes vertical charge transfer using an n well.

U.S. Pat. No. 5,210,433 to Ohsawa et al. describes a solid state CCD imaging device showing a potential well and a deep potential well for vertical charge

10   transfer.

U.S. Pat. No. 5,040,038 to Yutani et al. describes a solid state image sensor showing a transfer potential well under a transfer electrode.

15   U.S. Pat. No. 4,875,101 to Endo et al. describes a solid state imaging device showing shallow and deep potential wells for vertical charge transfer.

SUMMARY OF THE INVENTION

It is the objective of this invention to provide an Active Pixel Sensor structure which can control vertical charge transfer.

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This objective is achieved using a deep well structure. A silicon substrate having an epitaxial layer of p type silicon is provided. An N well of n type silicon is formed wherein the N well surrounds an island of p type silicon. A deep N well is formed of n type silicon underneath the island of p type silicon thereby forming a P well of p type silicon. The P well is within the boundaries of the N well and above the deep N well. The edges of the deep N well contact the bottom of the N well forming an overlap region which can either electrically connect the N well to the deep N well or electrically isolate the N well from the deep N well. N regions formed in the P well and P regions formed in the N well are used to reset the pixel and to read the pixel after a charge integration period. The overlap region can be used to connect the N well to the deep N well so that carriers generated in the deep N well can be transferred to the N well. The overlap region can also be depleted to isolate the N well from the deep N well so that charges transferred from the deep N well to the N well can be stored in the N well.

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Alternatively, a silicon substrate having an epitaxial layer of n type silicon is provided. A P well of p type silicon is formed wherein the P well surrounds an island of n type silicon. A deep P well is formed of p type silicon underneath the island of n type silicon thereby forming an N well of n type silicon. The N well is within the

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boundaries of the P well and above the deep P well. The edges of the deep P well contact the bottom of the P well forming an overlap region which can either electrically connect the P well to the deep P well or electrically isolate the P well from the deep P well. P regions formed in the N well and N regions formed in the P well are used to reset the

5   pixel and to read the pixel after a charge integration period. The overlap region can be used to connect the P well to the deep P well so that carriers generated in the deep P well can be transferred to the P well. The overlap region can be depleted to isolate the P well from the deep P well so that charges transferred from the deep P well to the P well can be stored in the P well.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 shows a cross section view of the active pixel sensor of this

5   invention.

Fig. 2 shows a top view of the active pixel sensor of this invention.

Fig. 3 shows a cross section view of two pixels joined by a single deep N

10   well or deep P well.

Fig. 4 shows a top view of a portion of an array of active pixel sensors of

this invention.

15   Fig. 5 shows a cross section view top view of a portion of an array of

active pixel sensors of this invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

5   Fig. 1 shows a cross section view of the Active Pixel Sensor of this

invention. In the first embodiment an N well 14 of n type silicon is formed in a p type

epitaxial silicon substrate 10. A deep N well 12 is formed a distance below the surface of

the substrate 10 thereby forming a P well 22 within the N well 14 and above the deep N

well 12. A overlap region 24 connects the N well 14 and the deep N well 12. The

overlap region 24 is designed such that the overlap region 24 will be depleted or not

10   depleted depending on the potential of the P Well 22. A first N region 16 and a second

N region 18 are formed in the P well 22. A P region 20 is formed in the N well 14.

            In the operation of the pixel the N well 14 is set at a reset voltage and the

P well 22 is set at a positive potential so that the overlap region 24 is not depleted. This

15   sets the potential of the deep N well 22 at the same potential as the N well 14. The

potential of the P well is then set to a negative potential so that the overlap region 24 is

depleted. This isolates the deep N 12 well during the charge integration period. After the

charge integration period has been completed the potential of the P well 22 is set to a

positive potential, the overlap region 24 is not depleted, and the charge accumulated by

20   the deep N well 12 is transferred to the N well. The potential of the P well 22 can be

adjusted to adjust the amount of depletion of the overlap region 24 and thereby control

the charge transfer to the N well 14.

In one mode of operation the potential of the N well 14 can be read before and after the transfer of the charge from the deep N well 12 to the N well 14 providing a pixel correlated double sampling operation.

5   The charge transfer from the deep N well 12 to the N well 14 is primarily determined by the P well 12 potential and the N well 14 potential. In another mode of operation the P well 22 could be left floating and the charge transfer would be controlled by adjusting the potential of the N well 14. In this case the P well 22 will be used in a manner similar to a floating gate sense node and the signal can be readout prior to,

10   during, and after the charge transfer from the deep N well 12 to the N well 14.

The previous example showed a single P well 22 formed in a single N well 14 with a deep N well 12. An overlap region 24 provides communication or isolation between the N well 14 and deep N well. A number of N wells with a single deep N well

15   can be used, having a P well formed in each of the N wells, and depletion regions to provide communication or isolation between each of the N wells and the deep N well. Fig. 3 shows a structure having two N wells, a first N well 34 and a second N well 36, having overlap regions connecting both N wells to the same deep N well 32. A P region 48 separates the two N wells. The first N well 34 is connected to the deep N well 32 by a

20   first overlap region 42. The second N well 36 is connected to the deep N well 32 by a second overlap region 44. There is a first P well 38 in the first N well 34 and a second P well 40 is the second N well 36. The overlap regions, 42 and 44, are designed to allow depletion of the first overlap region 42 while the second overlap region 44 is not

depleted, depletion of the second overlap region 44 while the first overlap region 42 is not depleted, depletion of both overlap regions, or leaving both overlap regions not depleted. During reset neither the first overlap region 42 nor the second overlap region 44 are depleted and the first N well 34, the second N well 36, and the deep N well 32 are

5   set to the same potential. This will reduce the kTC noise during reset. Binning of the first N well 34 and the second N well 36 can be accomplished by adjusting the potentials so that neither the first overlap region 42 nor the second overlap region 44 are depleted.

In the structures shown in Figs. 1 and 3, sufficiently high voltage is

10   applied to deplete the overlap regions; 24 in Fig. 1, and 42 and 44 in Fig. 3; during the charge integration period. After the integration period has been completed, charge transfer can be controlled by controlling the amount of depletion in the overlap regions; 24 in Fig. 1, and 42 and 44 in Fig. 3. In the structure shown in Fig. 3, the overlap regions, 42 and 44, can be turned on (not depleted) during the reset operation to connect

15   the N well regions, 36 and 38, to achieve reset noise suppression and turned off (depleted) after reset to isolate the N well regions, 36 and 38. In the structure shown in Fig. 3, the overlap regions, 42 and 44, can be turned on (not depleted) to connect adjacent N wells, 34 and 36, to achieve binning. In the structures shown in Figs. 1 and 3 the P well regions, 22 in Fig. 1 and 38 and 40 in Fig. 3, can be used as a floating gate sense

20   node for alternative non-destructive readout.

The above description has shown two N wells 34 and 36 which communicate by a single deep N well 32. As indicated above, a structure having a greater number of N wells and a single deep N well can also be used. In this case the N wells communicate to a single deep N well by means of a number of overlap regions.

5   Fig. 4 shows a top view and Fig. 5 shows a cross section view, taken along line 5-5' of Fig. 4, of an array of N wells 50 formed in a p type substrate 54 with a P well 50 in each of the N wells 52. A deep N well 56 in formed in the substrate 54 extending beneath each of the P wells 50. An overlap region 58 is formed between each of the N wells 52 and the deep N well 56. A first N region 51 and a second N region 53 are formed in each

10   P well 50. A P region 55 is formed in each N well 52. In this case a sufficiently high voltage is applied to deplete all of the overlap regions 58 during the charge integration period. After the charge integration period has been completed, charge transfer can be controlled by controlling the amount of depletion in each of the overlap regions 58. The overlap regions 58 can then be turned on during the reset operation to connect the

15   individual N wells 52 together, thereby achieving reset noise suppression. The overlap regions 58 will then be turned off after reset to isolate the N wells 52 for the next charge accumulation cycle. In this structure the overlap regions 58 are turned on to interconnect the N wells to achieve binning.

20   The overlap regions 58 are turned on during the reset cycle. The overlap regions 58 are then turned on during the charge integration period. After the completion of the charge integration period the overlap regions 58 can be used to control the charge transfer from the deep N well 56 to each of the N wells 52. The pixel is read by reading

the potential of the N wells 56. In one mode of operation the potential of the N wells 56

can be read before and after the transfer of the charge from the deep N well 56 to each N

well 56 providing a pixel correlated double sampling operation. The first 51 and second

53 N regions in each of the P wells 50 provide electrical communication to each of the P

5   wells 50. The P region in each of the N wells 52 provide electrical communication to

each of the N wells 52. The first N region 51, second N region 53, and P well 50 in each

N well 52 can be used as a floating gate field effect transistor. In this structure P well

regions 50 formed in each of the N wells 52 can be used as a floating gate sense node for

alternative non-destructive readout.

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        Those skilled in the art will readily recognize that the invention will also

work using a deep P well in an n type epitaxial silicon substrate. In this case n regions

are replaced by p regions, p regions are replaced by n regions positive potentials are

replaced by negative potentials, and negative potentials are replaced by positive

15   potentials.

        While the invention has been particularly shown and described with

reference to the preferred embodiments thereof, it will be understood by those skilled in

the art that various changes in form and details may be made without departing from the

20   spirit and scope of the invention.

        What is claimed is: